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Dr. John has been teaching and conducting research in computer architecture and digital systems design for almost two decades. She has coauthored DIGITAL SYSTEMS DESIGN USING VHDL and DIGITAL SYSTEMS DESIGN USING VERILOG and has edited several successful books on computer performance evaluation and workload characterization. She is an IEEE Fellow.

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The start signal starts the multiplication process. It loads the multiplicand (a) in a register and also loads the multiplier (b) in another register. Each D flip flop is controlled by a control signal. The DFFs shifts data to the right only when the control signal is high.

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